REMARKS/ARGUMENTS

Claims 1, 8 and 23 have been amended, and new claims 25-29 have been added, to more clearly define the invention. Accordingly, claims 1-4, 8 and 23-29 are pending in the application.

Claims 1-4, 8, 23 and 24 stand rejected under 35 U.S.C. § 102(e) over United States Patent Number 6,441,660 to Ingino, Jr. (Ingino). Applicant reserves the right to swear behind the Ingino reference. The present invention relates to a low injection charge pump. Claim 1 recites:

> A charge pump circuit comprising: a first plurality of serially connected transistors of a first conductivity type; a second plurality of serially connected transistors of a second conductivity type; said first plurality of serially connected transistors being serially connected to the second plurality of serially connected transistors; the interconnection of said first and second plurality of transistors providing an output adapted to be coupled to a load device; a gate of one of said first plurality of transistors being adapted to receive a $\overline{\text{DOWN}}$ pulse signal, a gate of another one of said first plurality of transistors being adapted to receive a DC bias signal, a gate of one of said second plurality of transistors being adapted to receive an UP pulse signal, and a gate of another one of said second plurality of transistors being adapted to receive another DC bias signal; and a first node at the interconnection of transistors of said first plurality of transistors being adapted to receive a DOWN pulse signal and a second node at the interconnection of transistors of said second plurality of transistors being adapted to receive an UP pulse signal. Emphasis added.

The Ingino reference relates to "[a] charge pump 18 ... coupled to receive ... level-shifted Up and Down signals from the level shifter 16 as well as a reference current I_{ref} from the current generator 30. The charge pump 18 provides an output voltage V_{Ctrl} to the VCO

20, and the loop filter 28 is coupled to the node between the charge pump 18 and the VCO 20 as well," (emphasis added). Column 3, line 11-16.

The Office Action alleges that V_{dummy} of Ingino teaches the claimed "output". To the contrary, however, only V_{Ctrl} is indicated to be an output of the Ingino circuit. "In response to an active Up signal, the charge pump 18 increases the charge on the output node, thus increasing V_{Ctrl}," (emphasis added). Column 5, lines 26-28. "Additionally, the charge pump 18 includes a series connection of transistors M_{d1}, M_{s1}, M_{d2}, and M_{c2} between the V_{Ctrl} output node and the V_{reg1} power supply." (emphasis added). Column 7, lines 22-24.

Nor does V_{Ctrl} teach or suggest the claimed "output,". because the transistors coupled to the V_{Ctrl} node of Ingino do not include "a gate of one of said first plurality of transistors being adapted to receive a $\overline{\text{DOWN}}$ pulse signal." Accordingly, Ingino does not teach or suggest every limitation of claim 1 including, "the interconnection of said first and second plurality of transistors providing an output adapted to be coupled to a load device." Therefore, the rejection of claim 1 under 35 USC § 102(e) over Ingino is overcome.

Claims 2-4 each depend directly from claim 1 and incorporate every limitation thereof. Accordingly, the rejection of claims 2-4 under 35 U.S.C. § 102(e) over Ingino is overcome for at least the reasons given above in relation to claim 1.

Claim 8 recites:

> A charge pump circuit comprising: a first plurality of serially connected transistors of a first conductivity type; a second plurality of serially connected transistors of a second conductivity type; said first plurality of serially connected transistors being serially connected to the second plurality of serially connected transistors; the interconnection of said first and second plurality of transistors providing an output adapted to be coupled to a load device; a gate of one of said

first plurality of transistors being adapted to receive a first switching signal, a gate of another one of said first plurality of transistors being adapted to receive a DC bias signal, a gate of one of said second plurality of transistors being adapted to receive a second switching signal, and a gate of the other of said second plurality of transistors being adapted to receive another DC bias signal; and a first node at the interconnection of transistors of said first plurality of transistors being adapted to receive a complementary first switching signal and a second node at the interconnection of transistors of said second plurality of transistors being adapted to receive a complementary second switching signal. Emphasis added.

As discussed above a relation to claim 1, the Ingino reference does not teach or suggest "a first plurality of serially connected transistors of a first conductivity type; a second plurality of serially connected transistors of a second conductivity type;...the interconnection of said first and second plurality of transistors providing an output adapted to be coupled to a load device," (emphasis added). Accordingly, Ingino does not anticipate the claimed invention or render it obvious, and the rejection of claim 8 under 35 U.S.C. § 102(e) over Ingino is overcome.

Claim 23 recites:

A method of operating a charge pump comprising: switching a first switching transistor in response to a first applied switching signal to affect an output at an output terminal adapted to be coupled to a load device; switching a second switching transistor in response to a second applied switching signal to affect an output at said output terminal; biasing the switching characteristics of said first and second switching transistors with bias transistors respectively serially connected to said first and second switching transistors; coupling a complementary signal of said first applied switching signal to a connection between said first switching transistor and an associated bias transistor; and coupling a complementary signal of said second applied switching signal to a

connection between said second switching transistor and an associated bias transistor. Emphasis added.

As discussed above in relation to claims 1 and 8, the Ingino reference does not teach or suggest, "[a] method of operating a charge pump comprising: switching a first switching transistor in response to a first applied switching signal to affect an output at an output terminal adapted to be coupled to a load device," (emphasis added). Accordingly, Ingino does not anticipate the claimed invention or render it obvious, and the rejection of claim 23 under 35 U.S.C. § 102(e) over Ingino is overcome.

Claim 24 depends directly from claim 23 and incorporates every limitation thereof. Accordingly, the rejection of claim 24 under 35 U.S.C. § 102(e) over Ingino is overcome for at least the reasons given above in relation to claim 23.

New claims 25-29 are believed to be patently distinguishable over the prior art and are thus in immediate condition for allowance.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully ~~submitted~~,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please amend claims 1, 8 and 23 as follows:

1. (Twice Amended) A charge pump circuit comprising:

a first plurality of serially connected transistors of a first conductivity type;

a second plurality of serially connected transistors of a second conductivity type;

said first plurality of serially connected transistors being serially connected to the second plurality of serially connected transistors;

the interconnection of said first and second plurality of transistors providing an output adapted to be coupled to a load device;

a gate of one of said first plurality of transistors being adapted to receive a $\overline{\text{DOWN}}$ pulse signal, a gate of another one of said first plurality of transistors being adapted to receive a DC bias signal, a gate of one of said second plurality of transistors being adapted to receive an UP pulse signal, and a gate of another one of said second plurality of transistors being adapted to receive another DC bias signal; and

a first node at the interconnection of transistors of said first plurality of transistors being adapted to receive a DOWN pulse signal and a second node at the interconnection of transistors of said second plurality of transistors being adapted to receive an $\overline{\text{UP}}$ pulse signal.

8. (Amended) A charge pump circuit comprising:

a first plurality of serially connected transistors of a first conductivity type;

a second plurality of serially connected transistors of a second conductivity type;

said first plurality of serially connected transistors being serially connected to the second plurality of serially connected transistors;

the interconnection of said first and second plurality of transistors providing an output adapted to be coupled to a load device;

a gate of one of said first plurality of transistors being adapted to receive a first switching signal, a gate of another one of said first plurality of transistors being adapted to receive a DC bias signal, a gate of one of said second plurality of transistors being adapted to receive a second switching signal, and a gate of the other of said second plurality of transistors being adapted to receive another DC bias signal; and

a first node at the interconnection of transistors of said first plurality of transistors being adapted to receive a complementary first switching signal and a second node at the interconnection of transistors of said second plurality of transistors being adapted to receive a complementary second switching signal.

23. (Thrice Amended) A method of operating a charge pump comprising:

switching a first switching transistor in response to a first applied switching signal to affect an output at an output terminal adapted to be coupled to a load device;

switching a second switching transistor in response to a second applied switching signal to affect an output at said output terminal;

biasing the switching characteristics of said first and second switching transistors with bias transistors respectively serially connected to said first and second switching transistors;

coupling a complementary signal of said first applied switching signal to a connection between said first switching transistor and an associated bias transistor; and

coupling a complementary signal of said second applied switching signal to a connection between said second switching transistor and an associated bias transistor.